UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,557	05/18/2005	Klaas-Jan De Langen	US02 0456 US	7465

24738 7590 04/20/2007

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
TABLER, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2809	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,557	DE LANGEN ET AL.	
	Examiner	Art Unit	
	Matthew C. Tabler	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 05.18.2005
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application #10/535,557 filed on May 18th, 2005 by Langen et al. under assignee Koninklijke Philips Electronics. This application is a 371 of PCT/IB03/05177 filed on November 15th, 2003. Currently, claims 1-20 are pending.

Priority

It is noted that this application appears to claim subject matter disclosed in prior Application No. 60/427,422, filed 11/18/2002 and Application No. 60/499,197, filed 8/28/2003. A reference to the prior application must be inserted as the first sentence(s) of the specification of this application or in an application data sheet (37 CFR 1.76), if applicant intends to rely on the filing date of the prior application under 35 U.S.C. 119(e), 120, 121, or 365(c). See 37 CFR 1.78(a). For benefit claims under 35 U.S.C. 120, 121, or 365(c), the reference must include the relationship (i.e., continuation, divisional, or continuation-in-part) of all nonprovisional applications. If the application is a utility or plant application filed under 35 U.S.C. 111(a) on or after November 29, 2000, the specific reference to the prior application must be submitted during the pendency of the application and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior application. If the application is a utility or plant application which entered the national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the specific reference must be submitted during the pendency of the application and within the later of four months from the date on which the national stage commenced under 35 U.S.C. 371(b) or (f) or sixteen months from the filing date of the prior application. See 37 CFR 1.78(a)(2)(ii) and (a)(5)(ii).

This time period is not extendable and a failure to submit the reference required by 35 U.S.C. 119(e) and/or 120, where applicable, within this time period is considered a waiver of any benefit of such prior application(s) under 35 U.S.C. 119(e), 120, 121 and 365(c). A benefit claim filed after the required time period may be accepted if it is accompanied by a grantable petition to accept an unintentionally delayed benefit claim under 35 U.S.C. 119(e), 120, 121 and 365(c). The petition must be accompanied by (1) the reference required by 35 U.S.C. 120 or 119(e) and 37 CFR 1.78(a)(2) or (a)(5) to the prior application (unless previously submitted), (2) a surcharge under 37 CFR 1.17(t), and (3) a statement that the entire delay between the date the claim was due under 37 CFR 1.78(a)(2) or (a)(5) and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was unintentional. The petition should be addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

If the reference to the prior application was previously submitted within the time period set forth in 37 CFR 1.78(a), but not in the first sentence(s) of the specification or an application data sheet (ADS) as required by 37 CFR 1.78(a) (e.g., if the reference was submitted in an oath or declaration or the application transmittal letter), and the information concerning the benefit claim was recognized by the Office as shown by its inclusion on the first filing receipt, the petition under 37 CFR 1.78(a) and the surcharge under 37 CFR 1.17(t) are not required. Applicant is still required to submit the reference in compliance with 37 CFR 1.78(a) by filing an amendment to the first sentence(s) of the specification or an ADS. See MPEP § 201.11.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on May 18th, 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: In Figure 1, "L1" and "L2"; in Figure 2, "D3"; in Figure 6, "M30", "M31", and "Ibias"; in Figure 7, "Iin", "Vout", and "D"; in Figure 8, "Vmax", "Iin", "D3", "M2", and "Vout"; "M1", "M2", "M3", "M4", "M7", "M8", "M9", "M10", "M11", "M12", "M13", "M14", "M15", "M16", "M17", "M18", "M21", "M22", "M30", "M31", "M32, "M33", "Iin/Vin" and "Ibias"; in Figure 10, "M8" and "M35"; in Figure 12, "M13", "M14", "I2/2", "I1/2", and "Vout"; in Figure 14, "I21" and "I22"; in Figure 16, "I2-I1" and "Iout"; and Figure 17, "Iin" and "Vout".

2. The drawings are objected to because Figure 15 is not described in the specification.

3. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not

accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

1. The disclosure is objected to because of the following informalities: On page 1, line 25,"Nominally" should be changed to "Normally". Appropriate correction is required.

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

1. Claim [20] is objected to because of the following informalities: In claim [20], line 4, "the output node" should be changed to "the common output node". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims [2], [9], and [16]-[17] are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claim [2] recites the limitation "the same channel-type" in line 3. Claim [9] recites the limitation "the current corresponding to the input signal" in line 3. Claim [9] recites the limitation "the net current" in line 7. Claim [16] recites the limitation "the effects of gate-drain capacitance" in line 3. Claim [17] recites the limitation "the effects of gate-drain capacitance" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims [1]-[4] and [6]-[20] are rejected under 35 U.S.C. 102(e) as being anticipated by Singh et al. (US Patent 6,452,418) published on September 17th, 2002.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

2. In regard to claim [1], Singh et al. shows a level shifter (Figure 3) comprising: a pair of current mirrors (Pt1, Pt2, Pr1, Pr2) that are configured to couple an input signal (In) from a first system (310) to a common output node (Out) in a second system (320) that is isolated from the first system, and a pair of diodes (D1, D2) that are configured to decouple one of the pair of current mirrors (Pt1, Pt2, Pr1, Pr2) from the input signal (In) if a fault occurs (Column 2, lines 63-65). (Column 2, lines 40-57)

3. In regard to claim [2], Singh et al. shows the level shifter of claim 1, wherein the pair of current mirrors comprise transistors that are each of the same channel-type (p-type).

4. In regard to claim [3], Singh et al. shows the level shifter of claim 1, wherein the pair of diodes are further configured to split current from the input signal (In) to provide substantially half the current to each of the pair of current mirrors when the fault does not occur (Column 3, lines 31-37).

5. In regard to claim [4], Singh et al. shows the level shifter of claim 1, wherein a first current mirror of the pair of current mirrors (Pt1, Pt2) is supplied by a first reference voltage (Vdd1) of the first system (Column 2, lines 46-49), and a second current mirror of the pair of current mirrors (Pr1, Pr2) is supplied by a second reference voltage (Vdd2) of the second system (Column 2, lines 46-49).

6. In regard to claim [6], Singh et al. shows the level shifter of claim 1, further including a current generator (Idrive) that is configured to provide a compensation current between the first system and the second system, to minimize a net current flow between the first system and the second system (Column 3, lines 15-29).

7. In regard to claim [7], Singh et al. shows the level shifter of claim 1, further including a voltage source (B) that is configured to provide bias between the first system and the second system to minimize switching transients (Column 3, lines 1-2).

8. In regard to claim [8], Singh et al. shows a level shifter (Figure 3) for coupling an input signal (In) from a first system (310) to an output node (Out) in a second system (320) that is isolated from the first system (310), comprising: a current mirror (Pt1, Pt2) that is configured to mirror current corresponding to the input signal (In) to a load at the output node (Out) and a pair of diodes (D1, D2) that are configured to select a reference voltage from one of the first system

(310) and the second system (320) to provide a net current to the current mirror (Column 2, lines 58-65).

9. In regard to claim [9], Singh et al. shows the level shifter of claim 8 further including: at least one other current mirror (It is well within the scope of the reference to include other current mirrors as shown – Pt1, Pt2, Pr1, Pr2 in Figure 3) that is configured to mirror the current corresponding to the input signal (In) to at least one other load in at least one other system (It is well within the scope of the reference to include at least one other load in another system as shown in Figure 3), and at least one other diode (It is will within the scope of the reference to include at least one other diode for another system as shown in Figure 3), operably coupled to the pair of diodes (D1, D2) to form a diode network (D1, D2, ..., Dn) that is configured to select the reference voltage from one of the first system (310), the second system (320), and the at least one other system (additional system), to provide the net current to the current mirror (Column 2, lines 58-65). (Column 3, lines 45-50)

10. In regard to claim [10], Singh et al. shows the level shifter of claim 8, further including: a second current mirror (Pr1, Pr2) that is configured to mirror another current corresponding to an input from the second system (320) to an other load in the first system (310). (Column 2, line 58 – Column 3, line 2)

11. In regard to claim [11], Singh et al. shows the level shifter of claim 8, wherein the current mirror comprises P-channel transistors (p-type), a first diode (D1) of the pair of diodes (D1, D2) is arranged in series between a first supply voltage (Vdd1) of the first system (310) and the current mirror (Pt1, Pt2), and a second diode (D2) of the pair of diodes (D1, D2) is arranged in series between a second supply voltage (Vdd2) of the second system (320) and the current mirror

(Pr1, Pr2), so that the reference voltage corresponds to whichever of the first supply voltage (Vdd1) and the second supply voltage (Vdd2) is at a higher potential. (Column 2, lines 46-52)

12. In regard to claim [12], Singh et al. shows the level shifter of claim 8, wherein the current mirror comprises N-channel transistors (n-type), a first diode (D2) of the pair of diodes (D1, D2) is arranged in series between the current mirror (Nt1, Nt2) and a first ground voltage (G1) of the first system (310), and a second diode (D1) of the pair of diodes (D1, D2) is arranged in series between the current mirror (Nr1, Nr2) and a second ground voltage (G2) of the second system (320), so that the reference voltage corresponds to whichever of the first ground voltage (G1) and the second ground voltage (G2) is at a lower potential. (Column 2, lines 46-52)

13. In regard to claim [13], Singh et al. shows the level shifter of claim 8, further including a second current mirror (Nt1, Nt2) that is configured to mirror a second current corresponding to an inversion of the input signal (In) to provide a differential output (Out) in the second reference system (320). (Column 2, lines 58-60)

14. In regard to claim [14], Singh et al. shows the level shifter of claim 8, further including one or more bias transistors (Nt1, Nt2) that is configured to provide a bias current (Ibias) to the current mirror to enhance a switching speed of the current mirror (Column 3, lines 15-30).

15. In regard to claim [15], Singh et al. shows the level shifter of claim 8, further including cascade transistors (Nt1, Nt2) corresponding to each transistor in the current mirror (Column 2, lines 58-60).

16. In regard to claim [16], Singh et al. shows the level shifter of claim 15, further including one or more current-injecting (Iweak) transistors (Nr1 or Nr2) that are configured to reduce the

effects of gate-drain capacitance associated with one or more of the cascade transistors (Column 3, lines 24-30).

17. In regard to claim [17], Singh et al. shows the level shifter of claim 15, farther including one or more isolation transistors (Nr1 or Nr2) that is configured to decouple the effects of gate-drain capacitance associated with one or more of the cascade transistors from the input signal (Column 3, lines 24-30).

18. In regard to claim [18], Singh et al. shows the level shifter of claim 8, further including a current generator (Idrive) that is configured to provide a compensation current between the first system and the second system, to substantially minimize a net current flow between the first system and the second system (Column 3, lines 15-29).

19. In regard to claim [19], Singh et al. shows a method (Figure 3) of coupling an input signal (In) from a first system (310) to a common output node (Out) in a second system (320) that is isolated from the first system (310; Column 2, lines 40-57), comprising: coupling the input signal (In) to the common output node (Out) via a pair of current mirrors (Pt1, Pt2, Pr1, Pr2), and providing a pair of diodes (D1, D2) that are configured to decouple one of the pair of current mirrors (Pt1, Pt2, Pr1, Pr2) from the input signal (In) if a fault occurs (Column 2, lines 63-65).

20. In regard to claim [20], Singh et al. shows a method of coupling an input signal (In) from a first system (310) to a common output node (Out) in a second system (320) that is isolated from the first system (310; Column 2, lines 40-57), comprising: mirroring current (through Pt1, Pt2, Pr1, Pr2) corresponding to the input signal (In) to a load at the output node (Out) via a current mirror (Pt1, Pt2), and selecting a reference voltage (Vdd1, Vdd2) from one of the first

system (310) and the second system (320) via a pair of diodes (D1, D2), to provide a net current to the current mirror (Column 2, lines 58-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim [5] is rejected under 35 U.S.C. 103(a) as being obvious over Singh et al.

Singh et al. shows the level shifter of claim 4.

Singh et al. fails to show the level shifter of claim 4 further comprising a third diode that is configured to decouple the first current mirror from the common output node if the fault occurs.

Schrader teaches a third diode (Figure 2A – D1) that is configured to decouple the first current mirror (Q1P, Q2P) from the common output node (at I0) if the fault occurs.

It would have been obvious to one skilled in the art, at time invention was made, to use a third diode that is configured to decouple the first current mirror from the common output node if the fault occurs, in the invention of Singh et al., with the motivation that this diode ensures protection from parasitic currents to the base of the current mirror as known by those of ordinary skill in the art as having a reasonable expectation of success.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C.

102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Tabler whose telephone number is (571) 270-1567. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MCT
April 13, 2007

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER